Extraction

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Today's broadband access is moving towards PONs at 10Gb/s. This requires a burst-mode receiver to support the TDMA protocol used in its upstream path [1, 2]. Such a receiver consists of a burst-mode transimpedance amplifier (BM-TIA) which largely dictates the performance of the receiver and a burst-mode post-amplifier (BM-PA) that removes all dc-offsets present in the BM-TIA signal and regenerates the logical amplitude information.

A BM-TIA needs to adjust its gain on a burst-per-burst basis to ensure large dynamic range. Typically, a BM-TIA has two or three gain settings and the gain is switched during the preamble of each burst [2, 3]. This switching is accomplished by comparing the peak signal level (either the positive peak for non-inverting front-ends or the negative peak for inverting front-ends) to a series of references using comparators. Each time the signal crosses a reference, the gain is reduced. The gain switching stops when the signal level is small enough to pass through the front-end without distortion. Previous implementations show two major shortcomings. First, if the signal level has barely crossed a reference level the associated comparator may switch state very slowly. This is the minimal overdrive condition of a comparator and no clocking signal is available to speed up the switching. Secondly, noise peaks acquired after the preamble can toggle the comparator even if the signal without noise remains slightly above/below the reference for an inverting/non-inverting front-end. So there exists a range of optical power for which the gain setting might not have ended at the end of the preamble. Worse, the gain might switch during the data portion of a burst possibly leading to its loss.

To avoid this late switching a mechanism called gain locking is implemented for a BM-TIA with two gain states (high and low gain) [4]. Because the arrival of the burst relative to the reset pulse may be unknown in a PON, one cannot rely on the reset signal to lock the gain. Therefore, the implemented gain-locking mechanism does not use any additional external control signal (see Fig. 11.1.1). After the reset pulse the TIA is in its high-gain setting. The signal level of the burst is measured using a negative peak detector (PKD). This voltage is compared to two voltage references, V_{ref1} and V_{ref2}, where $V_{ref1} > V_{ref2}$ and spaced sufficiently apart. A timer is started when the peak detector voltage crosses V_{ref1}. If V_{ref2} is also crossed *ReduceGain* becomes high, indicating that the TIA gain must be reduced. *FreezeGain* becomes high at a predefined interval after *StartTimer* became high. This sets the gain corresponding to the current value of *ReduceGain* using the D-flipflop. The late or slow switching as described above can occur for both V_{ref1} and V_{ref2}. However, this no longer affects the gain setting of the TIA after the preamble. Indeed, late switching of V_{ref1} will freeze the gain setting of the TIA in its high gain setting (as the input level in this case is close to V_{ref1} and far from V_{ref2} no gain switching is necessary). Late switching of V_{ref2} does not impact the gain setting of the TIA as it already will have been frozen by the toggling of *FreezeGain*. Late switching of both V_{ref1} and V_{ref2} is impossible as long as these references are spaced sufficiently apart (a spacing above 100mV is a very safe value). Note that for optical powers corresponding to peak signal levels close to V_{ref2}, it may not be known a priori in which gain setting the TIA will end up. By properly choosing the gain in both settings and carefully selecting V_{ref2} it can be ensured that no significant distortion is introduced in either gain setting for this range of optical input power. All references used in the gain-switching mechanism are generated using replica TIAs to increase the robustness of the gain switching and locking mechanism against PVT variations.

voltage swing provided to the single-ended-to-differential converter (S2D) and the output buffer, a coarse threshold is extracted and fed to the current input of a dummy TIA using a transconductor (see Fig. 11.1.2). Its differential transconductance is roughly equal to $1/(2R_F)$, with R_F being the gain of the TIA. As shown in Fig. 11.1.2, this ensures that the output V_{DU} of the dummy TIA is located roughly halfway the peak output of the actual TIA. As in [3], the threshold could also have been set by directly feeding it to the S2D. The proposed topology however, has superior PSRR and CMRR as both paths to the inputs of the S2D are now equal. When the TIA is switched to its low gain setting the transconductance is switched as well to maintain $g_{mLG}R_F \approx 1/2$. V_{DU} is a coarse and possibly inaccurate threshold, because g_mR_F can never be made exactly equal to 1/2. However, this is no shortcoming because the remaining offset will be cancelled in the BM-PA.

A traditional peak detector as in [5] could not be used because of current gain degradation during reverse emitter-base bias conditions [6] and due to the limited supply voltage of 2.7V. Therefore, a new peak detector is implemented (Fig. 11.1.3). A comparator compares the input level to the acquired peak and controls switches Q1-Q2. While acquiring the peak, the bias current is steered towards the hold capacitance. When the peak level crosses the input level, Q1-Q2 are switched and I_{charge} is diverted to V_{dd}. Due to the finite delay δt of the comparator, an error is incurred on the detected peak. Resistor R_{hold} limits this error, because the voltage across the resistor during acquisition toggles the comparator before *PeakOut* has reached its minimum value. The filter at the input avoids acquiring ringing peaks. The replica structure M1-M2 reduces the feedthrough from *In* towards *PeakOut* after the peak has been acquired.

The 1.1×1.8mm^2 BM-TIA is fabricated in a 0.25µm SiGe BiCMOS technology. Figure 11.1.4 shows a micrograph of the chip. It consumes 400mW from a 2.7V supply. The TIA is mounted together with a PIN photodiode (capacitance 200fF, responsivity 0.75A/W @ 1550nm) in a butterfly package. Figure 11.1.5 shows the output waveforms of the TIA at the beginning of the burst for -10.3dBm and -5.8dBm average optical power. These measurements show that the gain locking happens within 4.5ns from the start of the burst. If the gain is switched, the threshold requires an additional 1.5ns to settle. For small signals the threshold setting is done before the gain locks. Figure 11.1.6 shows the BER performance of the TIA measured in continuous mode using a commercial limiting amplifier. At 5Gb/s and using a PRBS of 2^{10}-1, a sensitivity of -15dBm and a dynamic range of 15.5dB are measured. At 9.8Gb/s and using an 8B/10B encoded data sequence, a sensitivity of -14dBm and a dynamic range of 12.2dB are measured.

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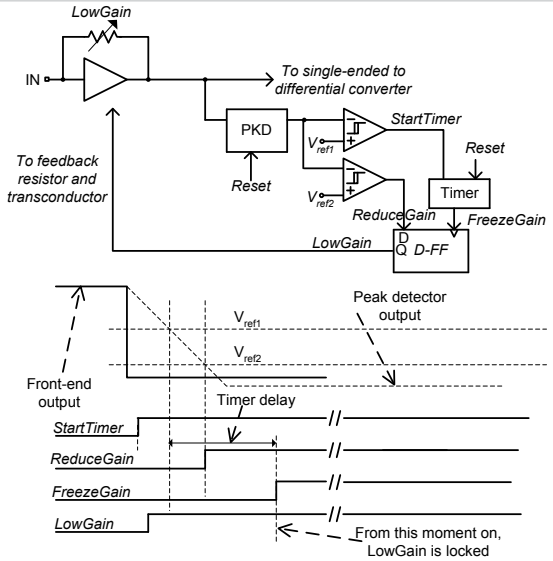

Figure 11.1.1: Gain-locking mechanism.

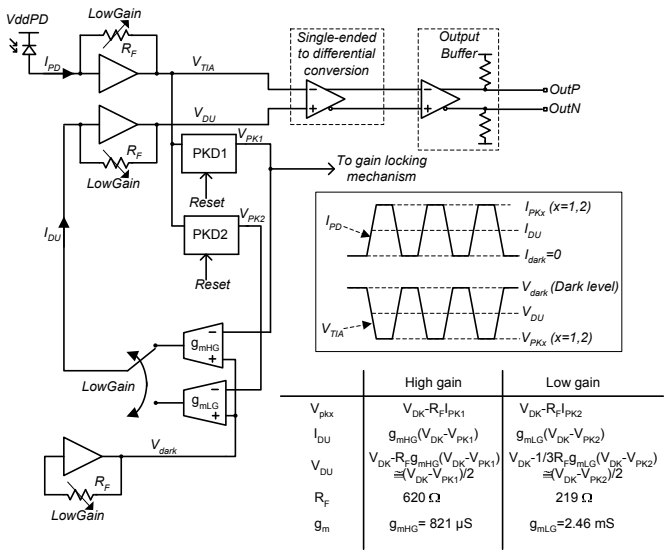

Figure 11.1.2: Top-level architecture.

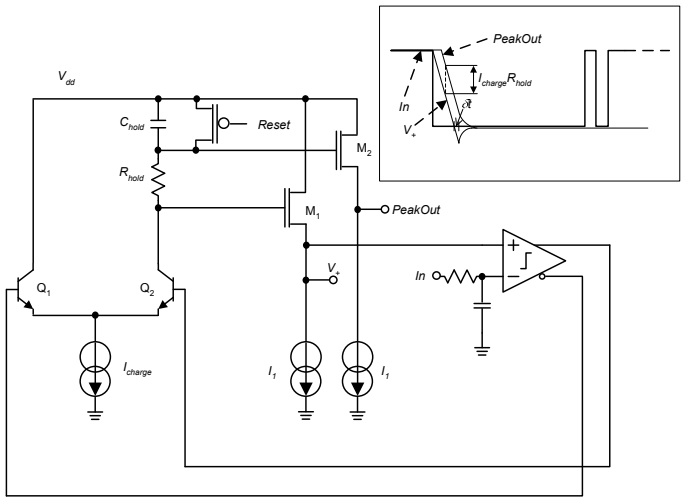

Figure 11.1.3: Switching peak detector.

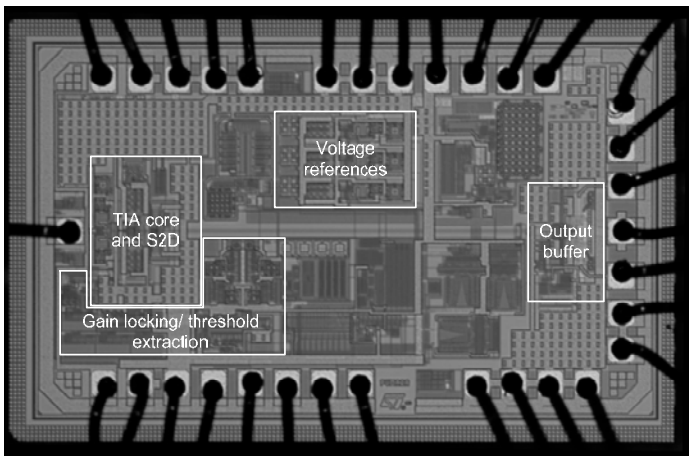

Figure 11.1.4: Die micrograph.

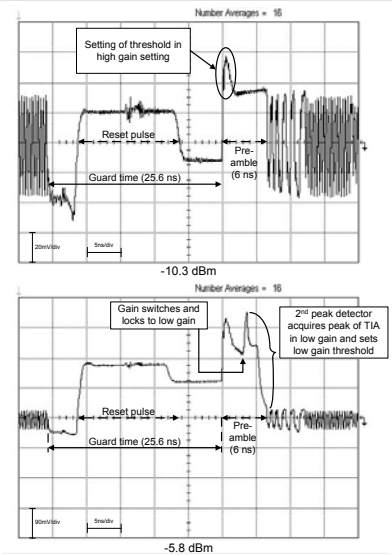

Figure 11.1.5: Gain-switching waveforms.

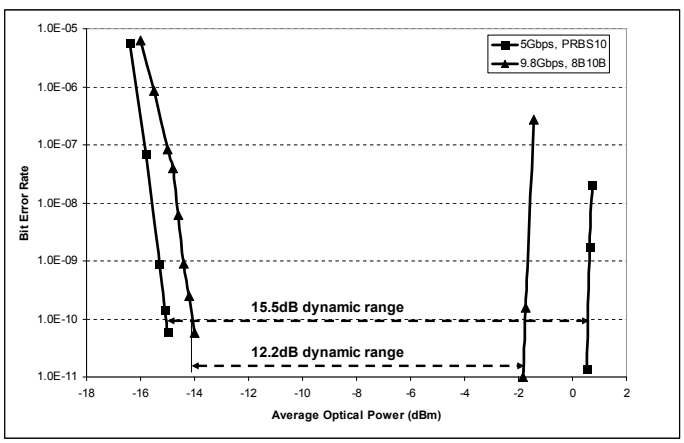

Figure 11.1.6: BER measurement results.